IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Cancelled)

2. (Currently amended): A processor comprising:

a set of general purpose registers; and

a set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers [when] during servicing of an exception [occurs], wherein said set of exception registers is substantially dedicated for servicing exceptions.

3. (Previously presented): The processor of Claim 2, wherein said set of exception registers is for servicing exceptions having a high priority not for those exceptions having a low priority.

4. (Original): The processor of Claim 2, wherein said processor provides a dedicated vector to said set of exception registers for said exception.

5. (Previously amended): The processor of Claim 2, wherein there are at least eight exception registers.

6. (Previously amended): The processor of Claim 2, wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls.

7. (Original): The processor of Claim 6, wherein said processor provides a first dedicated vector to software which uses said portion of said set of exception registers for interrupts and a second dedicated vector to software which uses said another portion of said set of exception registers for servicing operating system calls.

8. (Previously amended): The processor of Claim 2, further comprising:

a select logic circuit having a first input terminal that receives an exception register active bit and a second input terminal that receives a register address bit, said select logic circuit provides an output signal on an output terminal used to select between said set of general purpose registers and said exception registers.

9. (Cancelled).

10. (Previously amended): The method of Claim 12, wherein said at least one set of exception registers is a dedicated set of exception registers.

11. (Previously amended): The method of Claim 12, wherein servicing said exception using said at least one set of exception registers comprises modifying the values of the registers in said set of exception registers without disrupting the state of the interrupted task.

12. (Previously amended): A method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

swapping a set of general purpose registers for at least one set of exception registers if an exception asserted at said processor is a high priority exception;

servicing said exception using said at least one set of exception registers if said exception is a high priority exception;

preserving information from the set of general purpose registers in a memory if said exception is a low priority exception; and

swapping out said exception registers for said set of general purpose registers and resuming execution of said task if said exception is a high priority exception.

13. (Previously amended): The method of Claim 19, wherein said first vector is a dedicated vector and said providing said first vector automatically separates said high priority exception from said lower priority exceptions.

14. (Previously amended): The method of Claim 12, wherein said exception is a high priority exception and is either an interrupt or an operating system call, said method further comprising:

providing a first vector and activating at least a portion of said exception registers for said high priority exception when said exception is an interrupt;

providing a second vector and activating at least another portion of said exception registers for said high priority exception when said exception is an operating system call; and

providing a third vector and not activating said set of exception registers for lower priority exceptions.

15. (Original): The method of Claim 14, wherein said first vector and said second vector are dedicated vectors and said providing said first vector and providing said second vector automatically separates said high priority exception from said lower priority exceptions.

16. (Cancelled).

17. (Previously amended): An apparatus for executing tasks and servicing exceptions, said apparatus comprising:

means for interrupting a task when an exception is asserted;

means for servicing said exception without disrupting the state of the interrupted task, including means for activating at least one set of dedicated exception registers; and

means for resuming execution of said interrupted task, including means for deactivating said dedicated exception registers and activating general purpose registers to resume execution of said task.

18. (Original): The apparatus of Claim 17, wherein said means for activating comprises a first select logic circuit coupled to said set of general purpose registers and a second select logic circuit coupled to said at least one set of exception registers, said second select logic circuit receives an execution register active bit enabling said at least one set of exception registers and said second select logic circuit receives an inverted execution register active bit disabling said set of general purpose registers.

19. (Previously presented): The method of Claim 12 wherein said servicing comprises providing a first vector and activating said at least one set of exception registers for said high priority exception, and wherein said providing comprises providing a second vector and not activating said set of exception registers for lower priority exceptions.

20. (Previously presented): A processor comprising:

a set of general purpose registers; and

a set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when an exception having at least a predetermined priority level is detected by said processor and that are not switched when an exception having a priority less than the predetermined priority level is detected by said processor.

21. (Previously presented): The processor of Claim 20 further comprising another set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when another exception having at least said predetermined priority level is detected by the processor while said set if dedicated exception registers are switched for at least the subset of said set of general purpose registers.

22. (Previously presented): The processor of Claim 20 further comprising a select logic circuit having a first input that receives an exception register active bit and a second input that receives a register address bit, said select logic circuit provides an output signal on an output used to select between said set of general purpose registers and said exception registers.

23. (Previously presented): The processor of Claim 20 wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls.

24. (Previously presented): The processor of Claim 20 wherein said set of dedicated exception registers is switched only when an exception, of a first type, having at least a predetermined priority level is detected by said processor and the processor further comprising

another set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when another exception, of a second type, having at least said predetermined priority level is detected by the processor.